

THAT WHICH IS CLAIMED IS:

1. An electronic component comprising a two-way bus through which data elements travel in transit between peripherals and a central processing unit at the pace of a clock signal, wherein the central
5 processing unit and at least one of the peripherals each comprise a data encryption/decryption cell using one and the same secret key, a current value of said secret key being produced locally in each cell at each clock cycle from a random signal synchronous with the
10 clock signal and applied to each of the cells by a one-way transmission line.

2. An electronic component according to claim 1, wherein each cell comprises a shift register receiving said synchronous random signal as a data input and the clock signal as a clock input and
5 delivering, at output, a current secret key value at each clock cycle.

3. An electronic component according to claim 2, wherein said shift register is of the feedback type.

4. An electronic component according to claim 3, wherein the corresponding polynomial function of the register is irreducible.

5. An electronic component according to one of the claims 1 to 4, wherein each encryption/decryption cell comprises an encryption module receiving, as inputs, the current value of the secret key and a data element to be transmitted on the bus to give an encrypted data element at output and a decryption module receiving, as inputs, the current value of the secret key and a data element received

from the bus to deliver a decrypted data element at
10 output.

6. An electronic component according to
claim 5, wherein the encryption/decryption cell of the
central processing unit furthermore comprises a
conditional circuit to apply the current value of the
5 secret key or a neutral key to said encryption and
decryption modules according to an encryption enabling
signal given by a circuit for decoding the address of
the component.

7. An electronic component according to
claim 5 or 6, wherein the encryption module and the
decryption module use the same mathematical function.

8. An electronic component according to any
of the above claims, wherein a generator of said
synchronous random signal comprises a consumption
masking circuit.

9. An electronic component according to
claim 8, wherein said generator comprises a D type
flip-flop circuit receiving a random binary signal as
an input and the clock signal from the bus at the clock
5 input to give the synchronous random signal at output,
and wherein the consumption masking circuit is
connected between the output of said flip-flop circuit
and the transmission line.

10. An electronic component according to any
of the above claims, wherein said synchronous random
signal transmission line is set at zero by default by
the central processing unit, a generator of this signal
5 comprising a logic circuit to transmit said synchronous
random signal on the transmission line only after the

activation of a control signal by the central processing unit.

11. A system comprising an electronic component according to any of the foregoing claims.